Physical Design Engineer

Writing a great physical design engineer resume is important because it is one of the first things a potential employer will see when they are considering you for a position. It is your opportunity to make a good first impression and sell yourself as the best candidate for the job.

If you're looking for inspiration when it comes to drafting your own physical design engineer resume, look no further than the samples below. These resumes will help you highlight your experience and qualifications in the most effective way possible, giving you the best chance of landing the physical design engineer job you're after.

Resume samples

Lavender Tunney

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Summary

I am a Physical Design Engineer with over 4 years of experience in the semiconductor industry. I have worked on various process nodes, from 28nm to 7nm, and have gained expertise in block-level and full-chip integration. I am also familiar with different types of memories (DRAM, SRAM, eMMC) and their interfaces (DDRx/LPDDRx). In addition to my technical skills, I am also an effective team player and have excellent communication skills.

Experience

Physical Design Engineer at Northrop Grumman, VA **Mar 2022 - Present**

- Reduced design cycle time by 10% through process improvements.
- Increased productivity by 15% due to automated scripts and tools development.
- Yield improvement of 2.5% for a total of $1M in annual savings.
- Decreaseddebug timeby 50%, allowingfor the releaseof products2 weeks earlierthan scheduled.
- Developeda new floorplanningalgorithmthat improvedroutingdensityby 20% while also reducingoverall routelengthsby 5%.
- This was implementedin the company's latestplace-and-route tool,used on all future designs.

Associate Physical Design Engineer at General Dynamics, VA **Sep 2018 - Mar 2022**

- Successfully completed the physical design of 4 SoC projects in 28nm technology with a team size of 12 people.
- Achieved timing closure for all projects within schedule and met all performance goals.
- Delivered 2 presentations on floorplanning and clock tree synthesis at company-wide PD meetings which were well received by the audience.
- Created new scripts to automate various aspects of block level placement, resulting in significant time savings for subsequent projects.
- Optimized existing place & route tools and methodologies to achieve better quality of results while reducing runtimes by up to 50%.
- Authored 5 technical articles that were published on EDA industry websites, garnering over 1000 views collectively.

Education

Bachelor of Science in Electrical Engineering at Virginia Tech, **Sep 2014 - May 2018**

VA
I have learned how to design, analyze, and troubleshoot electrical and electronic circuits and systems.

Skills

- VLSI
- Verilog or VHDL
- IC Design
- SoC (System on Chip) design
- Circuit Design and Analysis
- Layout tools like Cadence Virtuoso, Synopsys ICC2

Almendra Woolheater

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Summary

Over 4 years of experience as a Physical Design Engineer. Proficient in the use of EDA tools for place and route, timing closure, power analysis/optimization. Experienced in working with multi-site design teams on large SoC projects from netlist to GDSII delivery.

Experience

Physical Design Engineer at Analog Devices, GA **May 2022 - Present**

- Led the physical design of a 28nm chip with 20M gates and 10 power domains, achieving TTM in 9 months.
- Implemented an automated DRC/LVS flow which reduced verification time by 60%.
- Developed a custom script to extract timing information from STA reports, saving 2 hours per run.
- Created several process improvement documents that increased team productivity by 15%.
- Trained 3 new hires on the company's design flows and methodologies.

- Presented at two industry conferences on techniques for high-speed clock tree synthesis.

Associate Physical Design Engineer at Cadence Design Systems, GA **Aug 2018 - Mar 2022**

- Led the physical design of a 28nm SoC with 7M gates and 15 block instances, completing timing closure in 8 months.
- Defined and implemented novel floorplanning techniques to reduce chip area by 5% while simultaneously improving routability.
- Developed an automated clock tree synthesis (CTS) methodology that reduced CTS runtime from 2 days to 12 hours, while also increasing quality of results.
- Implemented power optimization strategies which lowered dynamic power consumption by 20% across all voltage corners without sacrificing performance or violating any design constraints.
- Authored multiple EDA tool features/patches including enhancements to Synopsys PrimeTime P&R for improved memory characterization accuracy.

Education

Bachelor of Science in Electrical Engineering at Georgia Institute of Technology **Aug 2013 - May 2018**

Some skills I've learned are reading and understanding electrical schematics, using various test equipment, and soldering.

Skills

- VLSI
- Verilog/VHDL
- SoC Design
- RTL Coding
- Logic Synthesis
- Timing Analysis / STA
- Physical Implementation

Related Resume Samples

- Physical Therapist Aide
- Physical Therapy Aide
- Physical Therapy Assistant
- Physical Therapy Technician
- Physical Therapist Assistant
- Physical Education Teacher